Kenneth J. Baker

11705 SE 203rd St.
Kent, WA 98031-1698
253-859-9223
kbaker@nwlink.com

Objective To create complex digital ASICs.

Summary 21 years developing digital CMOS ASICs including fabrication of eleven different IC's. Areas of expertise include VHDL, 'e', logic design, verification, and synthesis.

Experience

Comtech EfData, Moscow, ID (Jan 2007 to Present).
Sr. Staff Design Engineer [remote from Kent, WA]

• Developed WAN optimization feature (DRE) for satellite communication systems using a combination of software and a PCI Express card. Created compression algorithm, architected hardware and software. Coding and verifying VHDL for FPGA as well as writing C++ application code.

• Designed, coded, and verified scatter-gather DMA system for an FPGA that maximized bandwidth between a PCIe bus and a custom compression ASIC.

Consultant, Kent, WA (Jan 2005 to Dec 2006).

• Created detailed block-level design documents and verification plans for dynamic Huffman encoder inside 0.12μ GZIP compression ASIC. Designed, coded and verified several VHDL blocks in the same chip.

Philips Ultrasound (Philips Medical Systems), Bothell, WA. (Oct. 1998 to Dec. 2004) Principal Design Engineer.

• Designed digital portion of high voltage mixed signal ASIC. Performed top-level layout of test chip.

• Led verification effort on 4 million gate 0.12μ beam-forming ASIC. Wrote top-level Verification Plan. Designed and implemented top-level verification environment using NcSim and Specman. Created reference models in 'e'. Developed methodology for using Functional Coverage to automatically check off Verification Plan items. Designed and coded VHDL interface blocks and performed block-level verification.

Philips Ultrasound - Continued

• Led team of six engineers developing a million gate 0.2μ ASIC. Developed front-end design flow for group. Wrote functional specification. Implemented receive beamforming function in VHDL. Created top-level testbench. Mentored fellow engineers.

• Adapted legacy Altera FPGA design to new system. Redesigned for robust operation and applied thorough verification techniques. Changes were rolled back into original design. Used Synplicity front end and Altera proprietary back end tools.

• Designed half of 400K gate signal processing ASIC (0.25μ). Wrote and implemented top-level verification plan. Introduced code coverage tools into project flow.

Advanced Hardware Architectures Inc., Pullman, WA. (Jan. 1991 to July 1998) Staff Design Engineer

• Developed four data compression and three tape formatter/controller ASICs. Designs were std cell around a custom core or pure std cell. Individual tasks included design, coding in VHDL, verification, synthesis and post-layout timing verification. Design tasks included architecture and algorithm development. Controller designs involved evaluating hardware/software tradeoffs. Implemented complex read-after-write tape algorithms in hardware. Other designs included postcode encoders/decoders and DMA controllers. Supervised three engineers. US Patents 5,694,125 and 5,734,926.

Education

University of Idaho, Moscow, ID. Bachelor of Science degree in Electrical Engineering, December 1990. Elective courses included Digital Systems Engineering, Computer Organization, Digital Simulation and Modeling.

Tools	Logic Simulation	Mentor Modeltech, Cadence NcSim
	Logic Synthesis	Synopsys Design Compiler, Altera Quartus II
	Code Coverage	TransEDA Vnavigator
	Formal Verification	Synopsys Formality
	Programming languages	VHDL, Verilog, SystemVerilog, 'e' Perl, TCL, C++, C, and Pascal
	Documentation	MS Word, FrameMaker, Timing Designer, Visio, Latex
	Operating Systems	Linux, Solaris, HP-UX Windows, Mac OS X

Security Natural-Born U.S. Citizen.

Interests Bicycling, Bavarian Sport Sedans, Auto Racing (from NASCAR to Formula 1), Writing.

References Available on request.